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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,173	01/14/2004	Nian Yang	AMD-AF01210	4822
7	590 08/25/2004		EXAM	INER
WAGNER, MURABITO & HAO LLP			WILSON, SCOTT R	
Third Floor				
Two North Market Street			ART UNIT	PAPER NUMBER
San Jose, CA 95113			2826	
			DATE MAILED: 08/25/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/758,173	YANG ET AL.				
Office Action Summary	Examiner	Art Unit				
	Scott R. Wilson	2826				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a replif NO period for reply is specified above, the maximum statutory period.  Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailine earned patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may a reply be timely within the statutory minimum of thirty (30) days will apply and will expire SIX (6) MONTHS from e. cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on <u>14 January 2004</u> .						
2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This	This action is <b>FINAL</b> . 2b)⊠ This action is non-final.					
·	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4)  Claim(s) 1-20 is/are pending in the application.  4a) Of the above claim(s) is/are withdrawn from consideration.  5)  Claim(s) is/are allowed.  6)  Claim(s) 1-5,9-13 and 17 is/are rejected.  7)  Claim(s) 6-8,14-16 and 18-20 is/are objected to.  8)  Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9)⊠ The specification is objected to by the Examine 10)⊠ The drawing(s) filed on 14 January 2004 is/are Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11)□ The oath or declaration is objected to by the E	e: a) $\square$ accepted or b) $\boxtimes$ objected or drawing(s) be held in abeyance. See ction is required if the drawing(s) is object.	e 37 CFR 1.85(a). lected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some col None of:  1. Certified copies of the priority documents have been received.  2. Certified copies of the priority documents have been received in Application No  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)	·	(070,440)				
<ol> <li>Notice of References Cited (PTO-892)</li> <li>Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08 Paper No(s)/Mail Date</li> </ol>	4) Interview Summary Paper No(s)/Mail Da  5) Notice of Informal P  6) Other:					

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#### **DETAILED ACTION**

#### **Drawings**

The drawings are acceptable for examination purposes, but new formal drawings will be required when the claims are allowed.

#### Specification

The disclosure is objected to because of the following informalities:

On page 7, line 38, "second" should read "first".

On page 7, line 39, "first" should read "second".

On page 7, line 40, "second" should read "first".

On page 7, line 41, "first metal layer 23 and second metal layer 26" should read "second metal layer 23 and first metal layer 26".

On page 8, line 36, "426" should read "425".

On page 9, line 40, "426" should read "425".

On page 12, line 2, "gate" should read "drain".

On page 12, line 4, "704" should read "706".

On page 12, line 5, "gate" should read "drain".

Appropriate correction is required.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Countryman et al..

As to claim 1, Countryman et al., Figures 2 through 5, discloses a semiconductor structure comprising a pad area (20), and an electrostatic discharge protective device disposed below said pad area (col. 2, lines 46-47, and Abstract).

As to claim 2, Countryman et al., Figure 5, discloses (col. 3, lines 56-57) a first layer of metal (62) disposed above the substrate (32) wherein said electrostatic discharge protective device is disposed below said first layer of metal, and a second layer of metal (60) disposed above said first layer of metal.

As to claim 3, Countryman et al., Figure 5, discloses a dielectric layer formed between said first and second metal layers, as well as between the electrostatic discharge protective device (25) through (30), and the pad area (20), and a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layers.

As to claim 9, Countryman et al., Figure 5, discloses (col. 3, lines 63-65) that there may be additional metal layers between said first and second metal layers.

Claims 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Countryman et al..

As to claim 10, Countryman et al., Figures 2 through 5, discloses a pad area apparatus for a semiconductor structure comprising a substrate (32), a first layer of metal (62) disposed above said substrate, a second layer of metal (60) disposed over said first layer of metal, and an electrostatic discharge protective device disposed within said substrate (col. 2, lines 46-47, and Abstract).

As to claim 11, Countryman et al., Figure 5, discloses a dielectric layer formed between said first and second metal layers, as well as between the electrostatic discharge protective device (25) through (30), and the pad area (20), and a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layers.

### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Countryman et al. in view of applicants prior art. As to claim 4, Countryman et al. discloses the device of claim 3, as described above. Countryman et al. does not disclose expressly that said electrostatic discharge protective device comprises a transistor and a resistance. Applicant discloses that in the prior art, ESD protection can be provided by transistors and resistors (Specification, p. 2, lines 26-27). At the time of invention, it would have been obvious to a person of ordinary skill in the art to use transistors and resistors to provide ESD protection in the device of Countryman et al.. The motivation for doing so would have been dissipate high electrostatically generated currents in a manner known in the art. Therefore, it would have been obvious to combine applicants prior art with Countryman et al. to obtain the invention as specified in claim 4.

As to claim 5, Countryman et al., Figure 5, discloses that the via between first and second metal layers (62) and (60), respectively, comprises a plurality of vias.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Countryman et al. in view of applicants prior art. As to claim 12, Countryman et al. discloses the device of claim 11, as described above. Countryman et al. does not disclose expressly that said electrostatic discharge protective device comprises a transistor and a resistance. Applicant discloses that in the prior art, ESD protection can be provided by transistors and resistors (Specification, p. 2, lines 26-27). At the time of invention, it would have been obvious to a person of ordinary skill in the art to use transistors and resistors to provide ESD protection in the device of Countryman et al.. The motivation for doing so would have been dissipate high electrostatically generated currents in a manner known in the art. Therefore, it would have been obvious to combine applicants prior art with Countryman et al. to obtain the invention as specified in claim 12.

As to claim 13, Countryman et al., Figure 5, discloses that the via between first and second metal layers (62) and (60), respectively, comprises a plurality of vias.

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Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Countryman et al. in view of applicants prior art. Countryman et al., Figure 5, discloses an electrostatic discharge protective device disposed within a substrate below a pad area of a semiconductor structure. Countryman et al. does not disclose expressly that said electrostatic discharge protective device comprises a transistor and a resistance. Applicant discloses that in the prior art, ESD protection can be provided by transistors and resistors (Specification, p. 2, lines 26-27). At the time of invention, it would have been obvious to a person of ordinary skill in the art to use transistors and resistors to provide ESD protection in the device of Countryman et al.. The motivation for doing so would have been dissipate high electrostatically generated currents in a manner known in the art. Therefore, it would have been obvious to combine applicants prior art with Countryman et al. to obtain the invention as specified in claim 17.

#### Allowable Subject Matter

Claims 6-8, 14-16 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed device where the resistance is comprised of the individual vias, formed in parallel.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this

application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC)

at 866-217-9197 (toll-free).

srw

August 17, 2004

NATHAN J. FLYNN SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800